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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,238	03/25/2004	David Bordui	5087-081	9570

20575 7590 07/20/2006

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,238	BORDUI, DAVID	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 25 March 2004. These drawings are deemed acceptable for examination.

Specification

2. The abstract of the disclosure is objected to because of the following:

The abstract exceeds the maximum of 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 1-7, and 13 are objected to because of the following informalities:

As for claim 1, word "for" should be added between the word "method" and "storing" in the first line of the claim for clarity. Additionally, the word "filed" should be changed to "filled" (line 10 of the claim – page line number 11).

As for claim 13, Examiner requests Applicant reword the claim to read "The cache recited in claim 8, wherein said cache is in a thumb drive". This rewording is consistent with claim 18. Additionally this change will make the claim more clear, as the claim from which it depends (i.e. claim 1) is claiming a cache, not a drive.

Claims 2-7 are further objected to for inheriting the limitations of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 15 recite the limitation "said flash memory data" in line 7 and line 9 respectively of each claim. There is insufficient antecedent basis for these limitations in the claims. More specifically, the only data recited is data transmitted by the bus. There is no indication that this data is specifically associated with the flash.

Claim 8 recites the limitation "said USB" in line 11 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "said serial bus" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claims 9-14, and 16-20 are rejected for further inheriting the limitations of claims 8 and 15 respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-10, 12, 14-16, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (US Patent 5,644,539) hereinafter Yamagami and in further view of Nickel et al. (US PG Publication 2004/0044838 A1), hereinafter Nickel.

As for claim 1, Yamagami teaches a method for storing data that is transmitted from a host to a flash memory via a bus, said method utilizing a cache memory that has banks of memory, said flash memory being divided into sectors (referring to Fig. 25, the flash memory depicted in this figure comprises a plurality of sectors (erasure blocks) – as shown by example with element 141. Additionally, a buffer area is included (142) which is capable of transferring data to any of the sectors of flash memory – col. 21, lines 22-60. The buffer area (cache) is made up of volatile memory and can either be the size of one sector, or greater than one sector – col. 21, lines 47-60) said method comprising the steps of:

associating a bank of memory with a sector to which data has been transmitted (the buffer can transfer data to any of the sectors one at a time, therefore the system is capable of associating the buffer with one of the sectors as the transfer takes place (col. 21, lines 46-60)),

temporarily storing data transmitted to said flash memory in said associated bank of memory (col. 21, lines 28-39 – data is written to the buffer area prior to being transferred to the corresponding sector in flash memory), and

transmitting data from a memory bank to the associated sector in said flash memory when said memory bank has been filed to the capacity of said sector (col. 21, lines 47-60 – the buffer transfers the data stored in its sector to the sector of the flash memory one erasure block at a time—that is, the buffer can transfer the data to the flash once it contains enough data to fill one erasure block of flash. Also note, col. 13, line 31-55 describes the smallest unit of memory for transfer as being one erasure block (i.e. sector). Fig. 11 further helps to illustrate this point (Fig. 11 shows the correspondence of an erasure block to the sector of flash in Fig. 25)).

Though Yamagami teaches his cache memory as being volatile, he fails to specifically teach it as being composed of MRAM as recited in claim 1.

Nickel however teaches a non-volatile memory module for use in a computer system, which makes use of MRAM (paragraph 0007, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Yamagami to further include Nickel's memory module into his own storage device employing flash memory. By doing so, Yamagami would benefit by having a memory module system which is both portable and removable, hence enabling his memory to be inserted and removed from a computer system via "hotplugging", without the risk of losing the contents of the MRAM due to sudden power loss to the module as taught by Nickel in paragraphs 0005 and 0008, all lines.

As for claim 8, Yamagami teaches a cache located between a bus and a flash memory, said bus transmitting data faster than the rate at which data can be directly

stored in said flash memory, said flash memory being divided into sectors, said cache comprising:

a plurality of banks of memory, each bank having at least a capacity equal to the size of a sector in said flash memory (referring to Fig. 25, the flash memory depicted in this figure comprises a plurality of sectors (erasure blocks) – as shown by example with element 141. Additionally, a buffer area is included (142) which is capable of transferring data to any of the sectors of flash memory – col. 21, lines 22-60. The buffer area (cache) is made up of volatile memory and can either be the size of one sector, or greater than one sector – col. 21, lines 47-60),

means for determining to which sector of said flash memory data is destined, means for temporarily associating a bank of said memory with a sector of said flash memory to which data is destined (the buffer can transfer data to any of the sectors one at a time, therefore the system is capable of associating the buffer with one of the sectors as the transfer takes place (col. 21, lines 46-60) once it makes the determination as to which sector requires the updated data– Fig. 4 depicts the process of determining which sector requires an update – col. 6, lines 4-39),

means which stores data received from said bus in the associated bank (col. 21, lines 28-39 – data is written to the buffer area prior to being transferred to the corresponding sector in flash memory), and

means which transfers data from a memory bank to the associated sector of said flash memory when said memory bank is full (col. 21, lines 47-60 – the

buffer transfers the data stored in its sector to the sector of the flash memory one erasure block at a time—that is, the buffer can transfer the data to the flash once it contains enough data to fill one erasure block of flash. Also note, col. 13, line 31-55 describes the smallest unit of memory for transfer as being one erasure block (i.e. sector). Fig. 11 further helps to illustrate this point (Fig. 11 shows the correspondence of an erasure block to the sector of flash in Fig. 25)).

Though Yamagami teaches his cache memory as being volatile, he fails to specifically teach his it as being composed of MRAM as recited in claim 8. Additionally he fails to teach the bus as being specifically implemented with USB.

Nickel however teaches a non-volatile memory module for use in a computer system, which makes the use of MRAM (paragraph 0007, all lines). Additionally Nickel teaches his bus as being USB compatible in paragraph 0035, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Yamagami to further include Nickel's memory module into his own storage device employing flash memory. By doing so, Yamagami would benefit by having a memory module system which is both portable and removable, hence enabling his memory to be inserted and removed from a computer system via "hotplugging", without the risk of losing the contents of the MRAM due to sudden power loss to the module as taught by Nickel in paragraphs 0005 and 0008, all lines.

As for claim 15, Yamagami teaches a method of operating a cache located between a bus and a flash memory, said bus transmitting data faster than the rate at

which data can be stored in said flash memory, said flash memory being divided into sectors, said cache comprising:

a plurality of banks of memory, each bank having a size equal to at least the size of a sector in said flash memory (referring to Fig. 25, the flash memory depicted in this figure comprises a plurality of sectors (erasure blocks) – as shown by example with element 141. Additionally, a buffer area is included (142) which is capable of transferring data to any of the sectors of flash memory – col. 21, lines 22-60. The buffer area (cache) is made up of volatile memory and can either be the size of one sector, or greater than one sector – col. 21, lines 47-60),

said method comprising:

determining to which sector of said flash memory data is destined, temporarily associating a bank of said memory with a sector of said flash memory to which data is destined (the buffer can transfer data to any of the sectors one at a time, therefore the system is capable of associating the buffer with one of the sectors as the transfer takes place (col. 21, lines 46-60) once it makes the determination as to which sector requires the updated data– Fig. 4 depicts the process of determining which sector requires an update – col. 6, lines 4-39),

temporarily storing data received from said bus in the associated memory bank (col. 21, lines 28-39 – data is written to the buffer area prior to being transferred to the corresponding sector in flash memory), and

transferring data from an memory bank to the associated sector of said flash memory when said memory bank is filled with an amount of data equal to the size of said sector (col. 21, lines 28-39 – data is written to the buffer area prior to being transferred to the corresponding sector in flash memory), and means which transfers data from a memory bank to the associated sector of said flash memory when said memory bank is full (col. 21, lines 47-60 – the buffer transfers the data stored in its sector to the sector of the flash memory one erasure block at a time—that is, the buffer can transfer the data to the flash once it contains enough data to fill one erasure block of flash. Also note, col. 13, line 31-55 describe the smallest unit of memory for transfer as being one erasure block (i.e. sector). Fig. 11 further helps to illustrate this point (Fig. 11 shows the correspondence of an erasure block to the sector of flash in Fig. 25)).

Though Yamagami teaches his cache memory as being volatile, he fails to specifically teach his it as being composed of MRAM as recited in claim 15. Additionally he fails to teach the bus as being specifically USB.

Nickel however teaches a non-volatile memory module for use in a computer system, which makes the use of MRAM (paragraph 0007, all lines). Additionally Nickel teaches his bus as being USB compatible in paragraph 0035, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Yamagami to further include Nickel's memory module into his own storage device employing flash memory. By doing so, Yamagami would benefit by having a

memory module system which is both portable and removable, hence enabling his memory to be inserted and removed from a computer system via "hotplugging", without the risk of losing the contents of the MRAM due to sudden power loss to the module as taught by Nickel in paragraphs 0005 and 0008, all lines.

As for claim 2, Yamagami teaches the method recited in claim 1 wherein there are less banks of memory than there are sectors in said flash memory (referring to Fig. 25, the buffer can contain as few as one sector of memory, whereas the figure depicts 16 sectors of flash). Though Yamagami teaches his cache memory as being volatile, he fails to specifically teach his it as being composed of MRAM as recited in claim 2.

As for claim 5, Yamagami teaches the method recited in claim 1 wherein a data bank is disassociated from a sector in said flash memory when data from said bank is transmitted to the associated sector in said flash memory (the buffer is associated with the corresponding flash sector during transfer. Once the transfer is complete the buffer is no longer associated with that particular sector). Again he fails to specifically teach his it as being composed of MRAM as recited in claim 5.

As for claim 6, though Yamagami teaches a bus, he fails to teach implementing the bus with USB.

As for claim 7, Yamagami teaches the method in claim 1 wherein each memory bank is at least as large as a sector in said flash memory (the buffer can be the same size as each flash sector per the discussion presented in claim 1). As stated previously, he fails to specifically teach his it as being composed of MRAM as recited in claim 7.

As for claim 20, though Yamagami teaches his buffer as being volatile memory, he fails to specifically note that the buffer will not lose any data if power to said cache is lost.

In summary, Yamagami teaches his cache memory as being volatile, however he fails to specifically teach it as being composed of MRAM as recited in claims 2, 5, and 7. Nickel however teaches a non-volatile memory module for use in a computer system, which makes use of MRAM (paragraph 0007, all lines). Nickel additionally teaches his MRAM as being capable of storing data even if a sudden power loss occurs as recited in claim 20 (paragraph 0007, all lines). Lastly, Nickel teaches his memory bus as being compatible with Universal Serial Bus (USB) – paragraph 0035, all lines as recited in claim 6 .

It would have been obvious to one of ordinary skill in the art at the time of the invention for Yamagami to further include Nickel's memory module into his own storage device employing flash memory. By doing so, Yamagami would benefit by having a memory module system which is both portable and removable, hence enabling his memory to be inserted and removed from a computer system via "hotplugging", without the risk of losing the contents of the MRAM due to sudden power loss to the module as taught by Nickel in paragraphs 0005 and 0008, all lines.

As for claim 10, Yamagami teaches the cache recited in claim 8 including an embedded processor that receives and decodes commands received from said serial bus (Fig. 1, element 4 depicts a microcomputer which comprises an embedded processor to encode and decode commands from the bus to the memory).

Claims 9, 12, 14, 16, and 19 are rejected for the same reasons as claims 6, 2, 5, 2, and 5 respectively.

6. Claims 3-4, 11, 13, 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Yamagami (US Patent 5,644,539) and Nickel (US PG Publication 2004/0044838 A1), and in further view of Imura (US Patent 6,513,719 B1).

As for claim 3, both Yamagami and Nickel fail to teach the flash memory as comprising NAND flash memory. Additionally, both Yamagami and Nickel fail to teach the flash memory and MRAM memory as being in a thumb drive as recited in claim 4.

Imura however teaches a card-shaped storage device which includes NAND flash memory (col. 1, line 60 through col. 2, line 10). Additionally Imura teaches his entire memory system as being embedded within a memory stick (i.e. thumb drive) – same line reference. It would have been obvious to one ordinary skill in the art at the time of the invention for Yamagami to further include Imura's card-shaped memory device into his own storage device. By doing so, Yamagami would benefit by having a much smaller size, making it more portable, and mechanically robust (i.e. vibration proof) than other means of storing data as taught by Imura in col. 1, line 48 through col. 2, line 16.

Claims 11, 13, 17, 18 are rejected for the same reasons as claims 3, 4, 3, and 4 respectively.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Makuta et al. (US PG Publication 2002/0186589 A) teach a nonvolatile semiconductor memory device.

Change et al. (US PG Publication 2003/0120841 A1) teach a system and method of data logging.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

7/17/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER